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EXAMINER
LEE, SIU M

ART UNIT	PAPER NUMBER
2611	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/629,020	EZELL, R. WILLIAM	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12 and 17-23* is/are pending in the application.

4a) Of the above claim(s) *4, 10, 20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-9,12,17-19,22 and 23* is/are rejected.

7)☐ Claim(s) *5, 11, 21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2007* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Remarks

1. Applicant's arguments with respect to claims 1-12 and 17-23 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. Claims 17-22 are rejected under U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 17 to 22 recite a software embodied in a computer readable medium and when executed operable to perform; receive a digital value; determine a bit value for a selected bit of the digital value; select a tuning range for a transconductor based on the bit value; and tune the transconductor within the selected range based on any remaining bits in the digital value by selecting an additional bit of the digital value; and selecting a subrange within the range based on the value of the additional bit. Software per se, that is the description or expression of the program, is not physical “things.” They are neither computer components nor statutory processes, as they are not “acts” being performed. Therefore, software per se is a non-statutory functional descriptive material.

Note that amending claim 17 to recite ---computer readable medium storing software when executed, operable to perform--- in the preamble would overcome this rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-3, 6-9, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by Ganeshan et al. (US 6,977,542 B2).

(1) Regarding claim 1 and 23:

Regarding claim 1 and 23, Ganeshan et al. discloses a method for tuning a trans-conductor (trans-conductor circuit in figure 5) comprising receive a digital value (digital code from digital low pass filter 360 in figure 3, column 5, lines 61-64); determine a bit value for a selected bit of the digital value (the switch selector 520 in figure 5 receives the bit on path 515 and generate the control signals to switch 510-1 to 510-4, the switch selector 520 determines the bit value and use the bit value to generate the switch control signals, column 7, lines 19-21); selecting a tuning range (selected stage) for a transconductor based on the bit value (bit(s) received on path 306 is used to select

among the various trans-conductor stages, column 5, line 3 and column 6, lines 31-32); and tuning the transconductor within the selected range based on any remaining bits in the digital value (remaining bits are used to fine-tune the trans-conductance within the selected stages, column 6, lines 33-35) by selecting an additional bit of the digital value; and selecting a subrange within the range based in the value of the additional bit (as disclose in paragraph 0060 of the disclosure of instant application, digital module 512 may set a subrange within the tuning range based on the additional bits) (Ganeshan et al. also discloses using two bits select the trans-conductance stages, as shown in figure 6, four lines are shown corresponding to the four possible value 00, 01, 10 and 11 of the two bits, the position of each line generally depends on the transconductance value in the connected stage, by using an additional bits, it is obvious that the transconductance range can be break down into 4 subrange, thus by using an additional bit, a subrange within the range based can be selected, the remaining five bits (instead of six bits) will be used to fine tune the sub transconductance range, column 7, lines 36-42).

(2) Regarding claim 2:

Ganeshan et al. discloses a method wherein selecting the tuning range comprises selecting a resistor from a plurality of resistors (resistor Gm1 to Gm4 in figure 5, column 7, lines 13-18).

(3) Regarding claim 3:

Ganeshan et al. discloses a method wherein tuning the transconductor comprises converting the remaining bits into an analog signal (DAC 370 in figure 3

convert the remaining bit into an analog signal, column 5, lines 59-63) and tuning the transconductor based on the analog signal (column 5, lines 59-63).

(4) Regarding claim 6:

Ganeshan et al. discloses a method of tuning a transconductor wherein the transconductor is used to form a selected one of a filter (LPF 170 and digital tuning circuit 175 in figure 1, column 3, line 55-column 4, line 4).

(5) Regarding claim 7:

Ganeshan et al. discloses a transconductor circuit comprising:

a digital-to-analog module operable to receive a digital value and to determine a bit value for a selected bit of the digital value (DAC 370 and mirror transconductor circuit 310 in figure 3, mirror transconductor circuit 310 receives a digital value and determine the bit value of the selected bits for the selection of selected stage, column 6, lines 40-48);

a digital control module operable to select a tuning range for a transconductor based on the bit value (switch selector 520 in figure 5, column 7, lines 19-21); and

an analog control module operable to tune the transconductor within the selected range based on any remaining bits in the digital value (mirror transconductor circuit 310 in figure 3, column 6, lines 40-48);

wherein:

the digital-to-analog module is further operable to select an additional bit of the digital value (Ganeshan et al. also discloses when two bits are used to select the trans-conductance stages, as shown in figure 6, four lines are shown

corresponding to the four possible value 00, 01, 10 and 11 of the two bits, column 7, lines 36-40); and

the digital control module is further operable to select a subrange within the range based in the value of the additional bit (Ganeshan et al. also discloses using two bits select the trans-conductance stages, as shown in figure 6, four lines are shown corresponding to the four possible value 00, 01, 10 and 11 of the two bits, the position of each line generally depends on the transconductance value in the connected stage, by using an additional bits, it is obvious that the transconductance range can be break down into 4 subrange, thus by using an additional bit, a subrange within the range based can be selected, the remaining five bits (instead of six bits) will be used to fine tune the sub transconductance range, column 7, lines 36-42).

(6) Regarding claim 8:

Ganeshan et al. discloses a transconductor circuit wherein the digital control module is further operable to select the tuning range by selecting a resistor from a plurality of resistors (resistor Gm1 to Gm4 in figure 5, column 7, lines 13-18).

(7) Regarding claim 9:

Ganeshan et al. discloses a transconductor circuit wherein the digital-to-analog module is further operable to convert the remaining bits into an analog signal (DAC 370 in figure 3 convert the remaining bit into an analog signal, column 5, lines 59-63); and the analog control module is further operable to tune the transconductor based on the analog signal (mirror transconductor circuit 310 in figure 3, column 5, lines 59-63).

(8) Regarding claim 12:

Ganeshan et al. discloses a transconductor circuit wherein the transconductor is used to form a selected one of a filter (LPF 170 and digital tuning circuit 175 in figure 1, column 3, line 55-column 4, line 4).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 17-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ganeshan et al. (US 6,977,542 B2) in view of Choi (US 6,538,833 B2).

(1) Regarding claim 17:

Ganeshan et al. discloses a method for tuning a trans-conductor (trans-conductor circuit in figure 5) comprising receive a digital value (digital code from digital low pass filter 360 in figure 3, column 5, lines 61-64); determine a bit value for a selected bit of the digital value (the switch selector 520 in figure 5 recieves the bit on path 515 and generate the control signals to switch 510-1 to 510-4, the switch selector 520 determines the bit value and use the bit value to generate the switch control signals, column 7, lines 19-21); selecting a tuning range (selected stage) for a transconductor based on the bit value (bit(s) received on path 306 is used to select among the various trans-conductor stages, column 5, line 3 and column 6, lines 31-32); and tuning the

transconductor within the selected range based on any remaining bits in the digital value (remaining bits are used to fine-tune the trans-conductance within the selected stages, column 6, lines 33-35) by selecting an additional bit of the digital value; and selecting a subrange within the range based in the value of the additional bit (as disclose in paragraph 0060 of the disclosure of instant application, digital module 512 may set a subrange within the tuning range based on the additional bits) (Ganeshan et al. also discloses using two bits select the trans-conductance stages, as shown in figure 6, four lines are shown corresponding to the four possible value 00, 01, 10 and 11 of the two bits, the position of each line generally depends on the transconductance value in the connected stage, by using an additional bits, it is obvious that the transconductance range can be break down into 4 subrange, thus by using an additional bit, a subrange within the range based can be selected, the remaining five bits (instead of six bits) will be used to fine tune the sub transconductance range, column 7, lines 36-42).

Ganeshan et al. fails to discloses a software embodied in a computer readable medium operable to perform the steps of receiving a digital value; determining a bit value for a selected bit of the digital value; selecting a tuning range for a transconductor based on the bit value; and tuning the transconductor within the selected range based on any remaining bits in the digital value.

However, Choi discloses a software stored in a computer-readable medium that improves the frequency response in a preamplifier (column 8, lines 23-26).

It is desirable to implement the steps of receiving a digital value; determining a bit value for a selected bit of the digital value; selecting a tuning range for a transconductor

based on the bit value; and tuning the transconductor within the selected range based on any remaining bits in the digital value in software embodied in a computer readable medium because it reduce the production cost and reduce the power consumption of the system (column 8, lines 23-26). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teaching of Choi with the system of Ganeshan et al. to improve the power efficiency and lower the cost of the system.

(2) Regarding claim 18:

Ganeshan et al. further discloses wherein selecting the tuning range comprises selecting a resistor from a plurality of resistors (resistor Gm1 to Gm4 in figure 5, column 7, lines 13-18).

(3) Regarding claim 19:

Ganeshan et al. further discloses wherein tuning the transconductor comprises converting the remaining bits into an analog signal (DAC 370 in figure 3 convert the remaining bit into an analog signal, column 5, lines 59-63) and tuning the transconductor based on the analog signal (column 5, lines 59-63).

(4) Regarding claim 22:

Ganeshan et al. further discloses wherein the transconductor is used to form a selected one of a filter (LPF 170 and digital tuning circuit 175 in figure 1, column 3, line 55-column 4, line 4).

Allowable Subject Matter

3. Claims 13-16 are allowable.

Claims 5, 11 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 5, 11, 13-16 and 21:

Claims 5, 11 and 21 recites a method and circuit for tuning a transconductance comprises selecting the tuning range comprises selecting a gain for the first transconductor and a gain range for the second transconductor and producing an output current of the transconductor using an output current of the first transconductor and an output current of the second transconductor. The closest prior art, Ganeshan et al. (US 6,977,542 B2) shows a similar system, which adjust the transconductance of a filter. However, Ganeshan et al. fails to disclose a method and circuit that comprises selecting the tuning range comprises selecting a gain for the first transconductor and a gain range for the second transconductor and producing an output current of the transconductor using an output current of the first transconductor and an output current of the second transconductor. The distinct features renders claims 5, 11, 13 and 21 allowable.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hayashi et al. (US 6,388,510 B2) discloses a transconductance-capacitance filter system.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-3:30 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M. Lee
4/19/2007

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER